IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Masaki ISHIDAO et al.**

Group Art Unit: **2655**

Serial No.: **10/768,188**

Attention: **Petitions Attorney**
Derek L. Woods

Filed: **February 2, 2004**

Confirmation No.: **3660**

For: **SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF**

Attorney Docket Number: **032209**
Customer Number: **38834**

REQUEST FOR RECONSIDERATION OF PETITION UNDER 37 CFR §1.47(a)

Attorney Mr. Derek L. Woods
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

November 18, 2004

Sir:

This paper is filed in response to the Decision mailed August 18, 2004. Applicants request reconsideration of the decision based on the additional items provided herewith which address the deficiencies noted in the Decision.

The Decision mailed August 18, 2004 indicated the prior petition was deficient with respect to proof that the non-signing inventor cannot be reached or refuses to sign the oath or declaration after having been presented with the application.

A renewed statement of "Necessary information for the missing inventor" along with a copy of the mail sent to the missing inventor is attached hereto. As stated in the "Necessary information for the missing inventor", the declaration and power of attorney, assignment and a copy of the application were sent to the missing inventor's last known address. However, the mail was returned since there was no one at the inventor's last known address.

It is believed that the attached "Necessary information for the missing inventor" provides the necessary information for the petition to be granted under 37 CFR 1.47(a).

In the event that any additional information is required for a grantable petition, the petitions attorney is requested to telephone applicants' undersigned attorney. Furthermore, in the event that any fees are due with respect to this paper, please charge our Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

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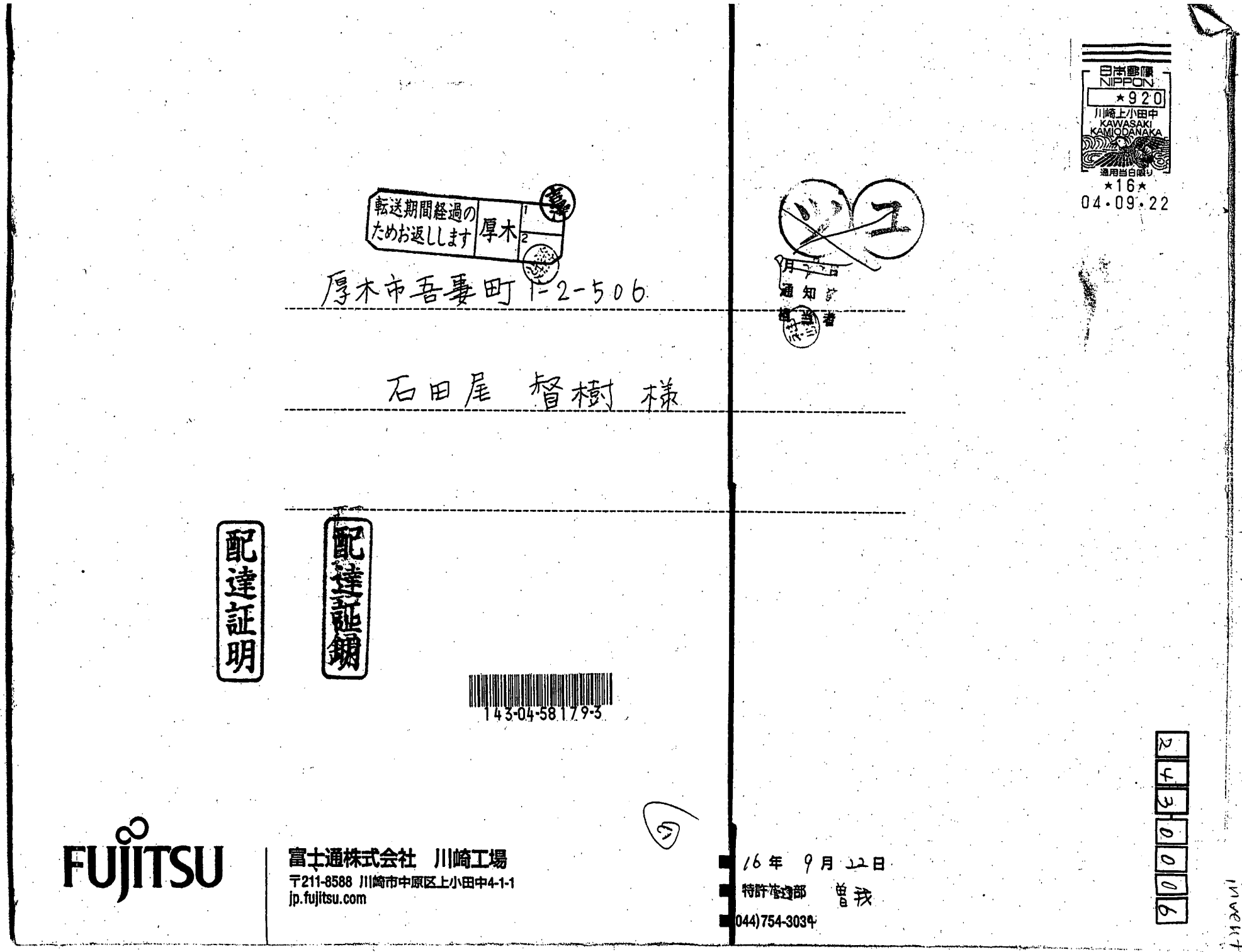
SGA/arf

Attachments: Necessary Information for the Missing Inventor with
Copy of mail sent to the missing inventor
Petition for Extension of Time



A copy of the mail sent to the missing inventor

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N171858

Docket No. _____ WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

Declaration and Power of Attorney for Patent Application
特許出願宣言書及び委任状
Japanese Language Declaration
日本語宣言書

私は、以下に記名された発明者として、ここに下記の通り宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先そして国籍は、私の氏名の後に記載された通りである。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明について、特許請求範囲に記載され、且つ特許が求められている発明主題に関して、私は、最初で、最先且つ唯一の発明者である（唯一の氏名が記載されている場合）か、或いは最初、最先且つ共同発明者である（複数の氏名が記載されている場合）と信じている。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

上記発明の明細書はここに添付されているが、下記の欄がチェックされている場合は、この限りでない：

the specification of which is attached hereto unless the following box is checked:

☐ _____の日に出願され、
この出願の米国出願番号または PCT 国際出願番号は、
_____であり、且つ
_____の日に補正された出願（該当する場合）

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、上記の補正書によって補正された、特許請求範囲を含む上記明細書を検討し、且つ内容を理解していることをここに表明する。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編規則１．５６に定義されている、特許性について重要な情報を開示する義務があることを承認する。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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私は、ここに、以下に記載した外国での特許出願または発明者証出願、或いは米国以外の少なくとも一国を指定している米国法典第３５編第３６５条(a)によるＰＣＴ国際出願について、同第１１９条(a)(b)項又は第３６５条(b)項に基づいて優先権の利益を主張するとともに、優先権を主張する本出願の出願日よりも前の出願日を有する外国で特許出願または発明者証出願、或いはＰＣＴ国際出願については、いかなる出願も、下記の枠内をチェックすることにより示した。

Prior Foreign Application(s)
外国での先行出願

		Priority Claimed 優先権主張	YES あり	NO なし
2003-027514 (Number) (番号)	Japan (Country) (国名)	February 4, 2003 (Day/Month/Year Filed) (出願日／月／年)	☑	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願日／月／年)	☐	☐

___他の優先権出願については添付のリスト参照

私は、ここに、下記のいかなる米国仮特許出願についても、その米国法典第３５編１１９条(e)項の利益を主張する。

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、ここに、下記のいかなる米国出願についても、その米国法典第３５編第１２０条に基づく利益を主張し、又米国を指定するいかなるＰＣＴ国際出願についても、その同第３６５条(c)に基づく利益を主張する。また、本出願の各特許請求の範囲の主題が、米国法典第３５編第１１２条第１段に規定された態様で、先行する米国出願又はＰＣＴ国際出願に開示されていない場合においては、その先行出願の出願日と本国内出願日またはＰＣＴ国際出願日との間の期間中に入手された情報で、連邦規則法典第３７編規則１．５６に定義された特許性に関る重要な情報について開示義務があることを承認する。

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、ここに表明された私自身の知識に係わる陳述が真実であり、且つ情報と信ずることに基づく陳述が、真実であると信じられることを宣言し、さらに、故意に虚偽の陳述などを行った場合は、米国法典第１８編第１００１条に基づき、罰金または拘禁、若しくはその両方により処罰され、またそのような故意による虚偽の陳述は、本出願またはそれに対して発行されるいかなる特許も、その有効性に問題が生ずることを理解した上で陳述が行われたことを、ここに宣言する。

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application for which priority is claimed.

	Priority Claimed 優先権主張	YES あり	NO なし
February 4, 2003 (Day/Month/Year Filed) (出願日／月／年)		☑	☐
(Day/Month/Year Filed) (出願日／月／年)		☐	☐

___ See attached list for additional prior foreign applications.

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Status: Patented, Pending, Abandoned)
(現況 ： 特許許可、係属中、放棄)

(Status: Patented, Pending, Abandoned)
(現況 ： 特許許可、係属中、放棄)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Docket No. _____ WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

Declaration and Power of Attorney for Patent Application
特許出願宣言書及び委任状
Japanese Language Declaration
日本語宣言書

委任状： 私は本出願を審査する手続を行い、且つ米国特許商標庁との全ての業務を遂行するために、記名された発明者として、下記の弁護士及び／または弁理士を任命する。

38834
米国特許商標庁

全ての通信は下記の住所へ送付されたい。

ウェスタマン、ハットリ、ダニエルズ＆エイドリアン,ＬＬＰ
１２５０ コネチカット通り N. W. スイート７００
ワシントンDC、２００３６

POWER OF ATTORNEY; As a named inventor, I hereby appoint The following attorney(s) and/or agent(s) to prosecute this Application and transact all business in the Patent and Trademark Office connected therewith.

38834
PATENT TRADEMARK OFFICE

Please direct all communications to the following address:

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 Connecticut Avenue, N.W., Suite 700
Washington, D.C. 20036

石田昌様のサインをお願いします

サインした日付をご記入ください

唯一または第一発明者氏名		Full name of sole or first inventor Masaki ISHIDAO
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Docket No. _____ Westerman, Hattori, Daniels & Adrian, LLP

U.S. ASSIGNMENT

(Insert ASSIGNEE's Name(s) Address(es))

IN CONSIDERATION of the sum of One Dollar ($1.00), and of other good and valuable consideration paid to the undersigned inventor(s) (hereinafter ASSIGNOR) by **FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8588 Japan**

(hereinafter ASSIGNEE), the receipt of which is hereby acknowledged, the undersigned ASSIGNOR hereby sells, assigns and transfers to ASSIGNEE the entire and exclusive right, title and interest to the invention entitled

(Title of Invention)

SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

(*If the assignment is being filed after the filing of the application, this section must be completed)

for which application for Letters Patent of the United States was executed on even date herewith unless otherwise indicated below:

* filed on _____ Serial No. _____

(Westerman, Hattori, Daniels & Adrian, LLP is hereby authorized to insert the series code, serial number and/or filing date hereon, when known)

and all Letters Patent of the United States to be obtained therefore on said application or any continuation, divisional, substitute, reissue or reexamination thereof for the full term or terms for which the same may be granted.

The ASSIGNOR agrees to execute all papers necessary in connection with the application and any continuation, divisional, reissue or reexamination applications thereof and also to execute separate assignments in connection with such applications as the ASSIGNEE may deem necessary or expedient.

The ASSIGNOR agrees to execute all papers necessary in connection with any interference, litigation, or other legal proceeding which may be declared concerning this application or any continuation, divisional, reissue or reexamination thereof or Letters Patent or reissue patent issued thereon and to cooperate with the ASSIGNEE in every way possible in obtaining and producing evidence and proceeding with such interference, litigation, or other legal proceeding.

石田尾様
フルネームサインを
お願いします

サインした
日付を
ご記入ください

IN WITNESS WHEREOF, the undersigned inventor(s) has (have) affixed his/her/their signature(s).

(Signatures)

X _____ X (Signature)	**Masaki ISHIDAO** (Type Name)	X _____ X (Date)
_____ (Signature)	**Masahiro KOBAYASHI** (Type Name)	_____ (Date)
_____ (Signature)	**Masatoshi FUKUDA** (Type Name)	_____ (Date)
_____ (Signature)	_____ (Type Name)	_____ (Date)
_____ (Signature)	_____ (Type Name)	_____ (Date)
_____ (Signature)	_____ (Type Name)	_____ (Date)

NO LEGALIZATION REQUIRED

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

Title :SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

Inventor(s) : Masaki ISHIDAO
Masahiro KOBAYASHI
Masatoshi FUKUDA

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2003-027514, filed on February 4, 2003, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[Field of the Invention]

The present invention relates to a semiconductor memory device suitable for a multi-value flash memory of which charge storage layers are spatially separated, and a manufacturing method thereof.

[Description of the Related Art]

Conventionally, there has been such a limitation in a multi-value flash memory that electron injection during write operation in a memory cell of MONOS (Metal/Oxide/Nitride/Oxide/Semiconductor) structure is possible only in the regions at both ends of a gate; thereby electrons which are injected into traps of a nitrided film are accumulated. These accumulated electrons cause a shift in a threshold voltage of a cell transistor. As a result, an electric current value of the cell transistor during read operation may vary to "1" or "0(zero)" in terms of information.

Generally, in such an element structure, such electrons as injected and held in a source side of

the cell transistor largely affect the shift of the threshold voltage of the cell transistor. Therefore, it is possible to obtain two bits of information, which is represented as four values: "00", "01", "10", and "11", in one memory cell by conducting read operation of the state of accumulated electrons of both ends of the gate twice at the source and at a drain by turns.

In a memory cell of conventional structure, there is placed a charge storing film, commonly a silicon nitride film, over the whole area of the gate, thereby charge redistribution may occur. The charge redistribution may vary the shifting amount of the threshold voltage and concurrently rewrite information of the other side of the gate, resulting in further readout error.

Accordingly, such an approach has been developed in order to prevent the charge redistribution that a charge storage layer is electrically divided into portions, and charge storing layers formed at both ends of the gate and a control gate are so formed as in a self-aligned manner. In this approach, charge is to be stored at both ends of the gate of the charge storage layers, so that charge redistribution is prevented by forming a separation oxide film.

In the prior art, when such a separation oxide film is formed, first, an oxide film as a material film of the separation oxide film, an oxide film for

an ONO film, and a polysilicon film (polycrystalline silicon film) for a gate electrode are formed sequentially on a tunnel oxide film. After that, the polysilicon film and the two oxide films are processed to take shape of a gate by anisotropic etching such as RIE (reactive ion etching) or the like. In the course of the process, overetching is conducted to the oxide films thereby an outer edge portion of the oxide film, which is used as the material film of the separation oxide film, is made retreat, so that the separation oxide film is formed.

A prior art is disclosed in Japanese Patent Laid-open No. 2001-168219.

SUMMARY OF THE INVENTION

After diligent efforts, the present inventors devised the following embodiment.

In a first semiconductor memory device relating to the present invention, a semiconductor substrate and a tunnel insulating film formed on the semiconductor substrate are provided. An Al_2O_3 film is formed, and further, a pair of charge storage layers sandwiching the Al_2O_3 film therebetween in plain view are formed on the tunnel insulating film. An insulating film is formed on the Al_2O_3 film and the pair of charge storage layers, and a gate electrode is formed on the insulating film. A source region and a drain region sandwiching the gate electrode in

plain view are formed as a pair on a surface of the semiconductor substrate.

A second semiconductor memory device relating to the present invention is intended for a semiconductor memory device having a pair of charge storage layers in each memory cell thereof and being capable of storing four values. Furthermore, an Al_2O_3 film insulating the pair of charge storage layers with each other is provided.

According to a manufacturing method of the semiconductor memory device relating to the present invention, first, a tunnel insulating film is formed on a semiconductor substrate, and an Al_2O_3 film, an insulating film, and a material film of a gate electrode are formed sequentially on the tunnel insulating film. After that, the gate electrode is formed by processing the material film of the gate electrode, the insulating film, and the Al_2O_3 film into a planar shape of the gate electrode, and an outer edge of the Al_2O_3 film is made retreat to be smaller than an outer edge of the gate electrode by performing isotropic etching to the Al_2O_3 film so as to form a pair of spaces under the insulating film. Subsequently, charge storage layers are respectively formed in the pair of spaces, and a source region and a drain region sandwiching the gate electrode in plain view are formed as a pair on the surface of the semiconductor substrate. Note that the tunnel

insulating film may be formed by oxidizing the surface of the semiconductor substrate, that is, the tunnel insulating film may be formed in any manner provided that the same is positioned on the semiconductor substrate in consequence. Also, the paired source and drain region may be formed before forming the charge storage layers to the extent that the material film of the gate electrode, the insulating film, and the Al_2O_3 film have been processed therebefore.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1F are sectional views showing a manufacturing method of a multi-value flash memory relating to an embodiment of the present invention sequentially by process;

Fig. 2 is a circuit diagram showing a configuration of a memory cell array of the multi-value flash memory; and

Fig. 3 is a graphical representation showing a relation between treatment solutions and corresponding etching rate of an Al_2O_3 film.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As described above, in a conventional method, an outer edge portion of the oxide film is made retreat by overetching. However, it is hard to control overetching amount in the course of RIE. In addition,

although thermal oxidation treatment is required, repeatability thereof among wafers or lots is insufficient in the aforementioned prior art due to the gate structure in which gate processing and heat treatment are extremely difficult to control. As a result, throughput and yield stay in a low level, and stability (reliability) in two-bit operation cannot be said satisfying as well.

An object of the present invention is to provide a semiconductor memory device capable of storing two bits of information per memory cell and a manufacturing method thereof, the semiconductor memory device enabling high throughput, yield, and reliability.

Hereinafter, concrete description of a semiconductor memory device and a manufacturing method thereof relating to an embodiment of the present invention will be given with reference to the accompanying drawings. Note that a configuration of each memory cell will be described here with the manufacturing method thereof for convenience. Figs. 1A to 1F are sectional views showing a manufacturing method of a multi-value flash memory (semiconductor memory device) relating to the embodiment of the present invention sequentially by process.

According to the present embodiment, as shown in Fig. 1A, first, a tunnel insulating film (tunnel oxide film) 2, an Al_2O_3 film 3, a silicon oxide film 4,

a polysilicon film (polycrystalline silicon film) 5, and a cap film 6 are formed sequentially on a semiconductor substrate, for example, a silicon substrate 1. The tunnel oxide film 2 has a thickness for example of 3 nm to 9 nm. The Al_2O_3 film 3 has a thickness for example of 5 nm to 15 nm. The silicon oxide film 4 has a thickness for example of 10 nm. The polysilicon film 5 has a thickness for example of 180 nm. Further, the cap film 6 is composed of a silicon oxide film or a silicon nitride film as an example.

Next, the cap film 6, the polysilicon film 5, the silicon oxide film 4, and the Al_2O_3 film 3 are patterned into a planar shape of a gate electrode. As a result, a gate electrode is configured by the polysilicon film 5. After that, ion injection is performed using the patterned cap film 6 and the like as a mask to form for example n^- diffusion layers 7 on a surface of the silicon substrate 1.

As shown in Fig. 1B, thereafter, isotropic etching of the Al_2O_3 film 3 is performed to retreat an outer edge of the Al_2O_3 film 3 to be smaller than that of the gate electrode (patterned polysilicon film 5). In the isotropic etching, a solution of sulfuric acid with hydrogen peroxide is used as an example. The solution of sulfuric acid with hydrogen peroxide exhibits higher etching rate to the Al_2O_3 film 3, while the silicon oxide film, the silicon nitride

film, the polysilicon film, and the like are hardly removed, enabling almost exclusive etching of the Al_2O_3 film 3 at a high selectivity ratio.

Subsequently, as shown in Fig. 1C, a conductor film, which is capable of holding an electron that is injected thereinto from a channel, is formed all over surface. According to the present embodiment, as an example of such a conductor film, a polysilicon film 8 is formed. In the formation, the polysilicon film 8 is formed to fill spaces under the silicon oxide film 4, the spaces being formed when the Al_2O_3 film 3 is made retreat. Such a polysilicon film 8 can be formed, for example, by atmospheric pressure CVD method.

Subsequently, as shown in Fig. 1D, the polysilicon film 8 is processed by anisotropic etching, for example, RIE so that the polysilicon films 8 each having a predetermined thickness (thickness in terms of not vertical direction but horizontal direction) are remained on the side portions of the polysilicon film 5 and the like. At this time, the polysilicon films 8 are also made remain in the spaces under the silicon oxide film 4, the spaces being formed when the Al_2O_3 film 3 is made retreat. The polysilicon films 8 to be remained on the side portions of the polysilicon film 5 and the like have the same thickness as of a sidewall for forming an LDD structure, as an example.

Subsequently, thermal oxidation method is performed to oxidize portions of the polysilicon films 8 except portions in the spaces formed under the silicon oxide film 4 when the Al_2O_3 film 3 is made retreat. Consequently, as shown in Fig. 1E, sidewall oxide films (sidewall insulating films) 9 are formed.

Subsequently, as shown in Fig. 1F, ion implantation is performed at a higher concentration ratio than that employed when the n^- diffusion layers 7 are formed to thereby form, for example, n^+ diffusion layers 10 on the surface of the silicon substrate 1 using the cap film 6 and the sidewall oxide films 9 as a mask. With the n^- diffusion layers 7 and the n^+ diffusion layers 10, a source and drain region of the LDD structure is configured.

After that, an interlayer insulating film, a contact hole, a wiring or the like are formed to complete the multi-value flash memory.

Fig. 2 is a circuit diagram showing a configuration of a memory cell array of the multi-value flash memory. The memory cell array is composed of a plurality of memory cells 11 arranged, the memory cells 11 being formed in the above-described manner. The gate of each memory cell 11 is connected to a word line 12, and the source and drain thereof are connected to bit lines 13.

As shown in Fig. 1F, in the multi-value flash memory configured in the above-described manner, the

Al_2O_3 film 3 is provided in each memory cell 11 in plain view, being sandwiched between the two polysilicon films 8 serving as charge storage layers, preventing charge from traveling between these polysilicon films 8. Hence, two-bit operation is stably performed and high reliability is obtained.

Further, the isotropic etching employed in the manufacturing method shows high selectivity ratio to the Al_2O_3 film 3; thereby size control of the spaces is extremely facilitated. Fig. 3 is a graphical representation showing a relation between treatment solutions and corresponding etching rate of the Al_2O_3 film. In the above-described embodiment, as shown in Fig. 3, the Al_2O_3 film 3 is isotropically etched using the solution of sulfuric acid with hydrogen peroxide (POS), and therefore, etching is conducted at a high rate. On the contrary, the silicon oxide film 4, the polysilicon oxide film 5, the cap film 6 and the like are hardly etched by the sulfuric acid with hydrogen peroxide. Consequently, the Al_2O_3 film 3 is etched at such a high selectivity ratio that etching amount can be placed under control with extreme ease, therefore throughput and yield are improved.

Note that, as shown in Fig. 3, the Al_2O_3 film can be etched at a high rate also by HCl, HNO_3, H_2O_2, H_2SO_4, and HF, whereas, HF cannot be for use therein since the use of HF concurrently removes the silicon oxide film. Although HCl, HNO_3, H_2O_2, and H_2SO_4 can be for

use, the solution of sulfuric acid with hydrogen peroxide (POS) is the most preferable one.

Additionally, according to the above-described embodiment, the sidewall oxide films 9 are formed by oxidizing parts of the polysilicon films 8; however, the method for forming a sidewall oxide film is not limited thereto. To cite a case, in the process as shown in Fig. 1D, the sidewall oxide film may be formed through deposition by atmospheric pressure CVD method or the like of the silicon oxide film and etch back thereof after anisotropic etching so performed as to leave the polysilicon films 8 only in the spaces formed under the silicon oxide film 4.

As detailed hereinbefore, according to the present invention, it is possible without fail to insulate a pair of charge storage layers with each other using an Al_2O_3 film, enabling stable two-bit operation. In addition, the etching of the Al_2O_3 film can be performed at a high selectivity ratio as compared to that of a polycrystalline silicon film, a silicon oxide film, and the like, facilitating the control of the etching amount with extreme ease. As a result, improvement of throughput and yield are enabled.

The present embodiments are to be considered in all respects as illustrative and no restrictive, and all changes which come within the meaning and range of equivalency of the claims are therefore intended

to be embraced therein. The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof.

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a tunnel insulating film formed on said semiconductor substrate;

an Al_2O_3 film formed on said tunnel insulating film;

a pair of charge storage layers sandwiching said Al_2O_3 film therebetween in plain view formed on said tunnel insulating film;

an insulating film formed on said Al_2O_3 film and said pair of charge storage layers;

a gate electrode formed on said insulating film; and

a source region and a drain region formed as a pair sandwiching said gate electrode in plain view formed on a surface of said semiconductor substrate.

2. The semiconductor memory device according to claim 1, further comprising a sidewall insulating film formed over a side surface of said gate electrode, said insulating film, and said pair of charge storage layers.

3. A semiconductor memory device having a pair of charge storage layers in each memory cell thereof and being capable of storing four values, comprising an Al_2O_3 film insulating said pair of charge storage layers with each other.

4. The semiconductor memory device according to claim 1, wherein

said charge storage layers are composed of a polycrystalline silicon.

5. The semiconductor memory device according to claim 3, wherein

said charge storage layers are composed of a polycrystalline silicon.

6. The semiconductor memory device according to claim 1, wherein

said tunnel insulating film has a thickness of 3 nm to 9 nm.

7. The semiconductor memory device according to claim 3, wherein

a tunnel insulating film has a thickness of 3 nm to 9 nm.

8. The semiconductor memory device according to claim 1, wherein

said Al_2O_3 film and said pair of charge storage layers have a thickness of 5 nm to 15 nm.

9. The semiconductor memory device according to claim 3, wherein

said Al_2O_3 film and said pair of charge storage layers have a thickness of 5 nm to 15 nm.

10. A manufacturing method of a semiconductor memory device comprising the steps of:

forming a tunnel insulating film on a semiconductor substrate;

forming sequentially an Al_2O_3 film, an insulating film, and a material film of a gate electrode on the tunnel insulating film;

forming a gate electrode by processing the material film of the gate electrode, the insulating film, and the Al_2O_3 film into a planar shape of the gate electrode;

making a retreat of an outer edge of the Al_2O_3 film to be smaller than an outer edge of the gate electrode by performing isotropic etching to the Al_2O_3 film so as to form a pair of spaces under the insulating film;

forming charge storage layers respectively in the pair of spaces; and

forming a source region and a drain region sandwiching the gate electrode in plain view, as a pair, on a surface of the semiconductor substrate.

11. The manufacturing method of the semiconductor memory device according to claim 10, wherein

isotropic etching of the Al_2O_3 film is performed using a solution of sulfuric acid with hydrogen peroxide during the step of performing isotropic etching to the Al_2O_3 film.

12. The manufacturing method of the semiconductor memory device according to claim 10, wherein

a polycrystalline silicon film is formed as the charge storage layers.

13. The manufacturing method of the semiconductor memory device according to claim 10, wherein

said step of forming the charge storage layers comprises the steps of:

forming a polycrystalline silicon film all over surface; and

making the polycrystalline silicon film remain in the spaces and forming a sidewall composed of the polycrystalline silicon film over side surfaces of the gate electrode and the insulating film by performing anisotropic etching to the polycrystalline silicon film.

14. The manufacturing method of the semiconductor memory device according to claim 13, wherein

said step of forming the charge storage layers comprises a step of oxidizing the sidewall after the step of performing anisotropic etching to the polycrystalline silicon film.

15. The manufacturing method of the semiconductor memory device according to claim 10, wherein

said step of forming the charge storage layers comprises the steps of:

forming a polycrystalline silicon film all over surface; and

making the polycrystalline silicon film remain only in the spaces by performing anisotropic etching to the polycrystalline silicon film.

16. The manufacturing method of the semiconductor memory device according to claim 15, wherein

said step of forming the charge storage layers comprises the steps of:

forming an insulating film for a sidewall all over surface; and

forming a sidewall insulating film over side surfaces of the gate electrode and the insulating film by etching back the insulating film for the sidewall, after the step of performing anisotropic etching to the polycrystalline silicon film.

17. The manufacturing method of the semiconductor memory device according to claim 10, wherein

the tunnel insulating film has a thickness of 3 nm to 9 nm.

18. The manufacturing method of the semiconductor memory device according to claim 10, wherein

the Al_2O_3 film and the pair of charge storage layers have a thickness of 5 nm to 15 nm.

19. The manufacturing method of the semiconductor memory device according to claim 11, wherein

the tunnel insulating film has a thickness of 3 nm to 9 nm.

20. The manufacturing method of the semiconductor memory device according to claim 11, wherein

the Al_2O_3 film and a pair of charge storage layers have a thickness of 5 nm to 15 nm.

ABSTRACT OF THE DISCLOSURE

A polysilicon film and the like are patterned to form n⁻ diffusion layers on a silicon substrate. Subsequently, an outer edge of an Al_2O_3 film is made retreat to be smaller than that of a gate electrode by performing isotropic etching of the Al_2O_3 film, using a solution of sulfuric acid with hydrogen peroxide. A silicon oxide film, a silicon nitride film, the polysilicon film and the like are hardly removed although the solution of sulfuric acid with hydrogen peroxide exhibits higher etching rate to the Al_2O_3 film, enabling almost exclusive etching of the Al_2O_3 film at a high selectivity ratio. Subsequently, another polysilicon film is formed so as to fill spaces formed after the retreat of the Al_2O_3 film under the silicon oxide film. Subsequently, a sidewall insulating film is formed by remaining portions of the later polysilicon film in the spaces by performing RIE, oxidation, or the like of the later polysilicon film.

FIG. 1A

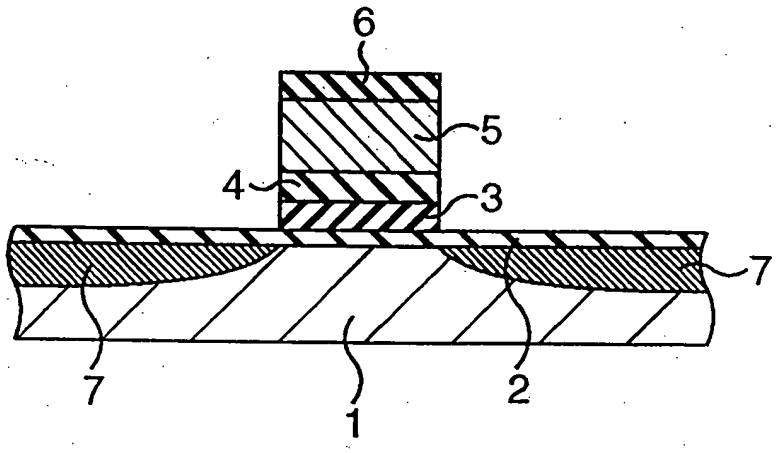


FIG. 1B

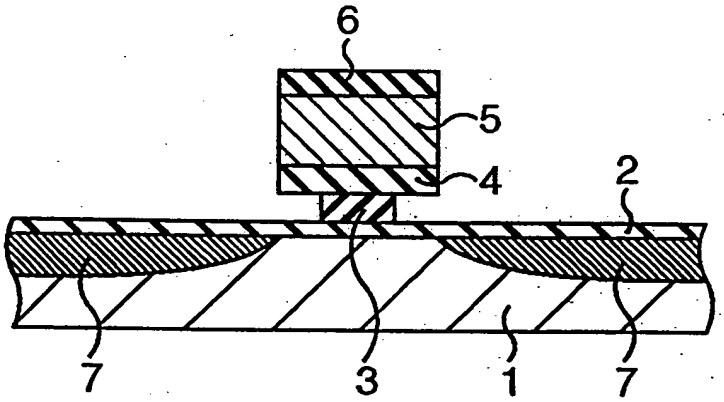


FIG. 1C

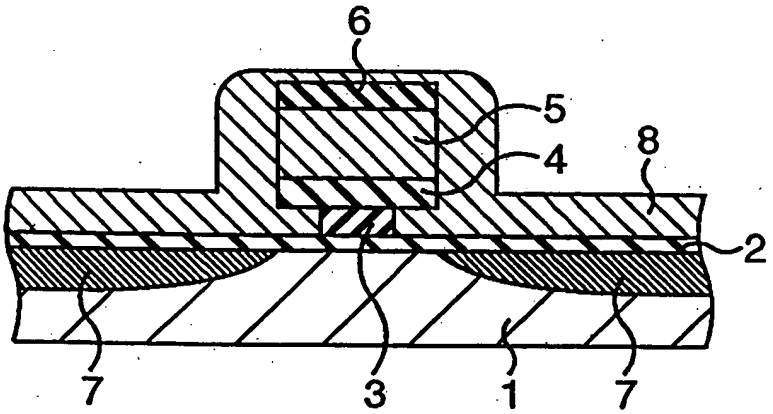


FIG. 1D

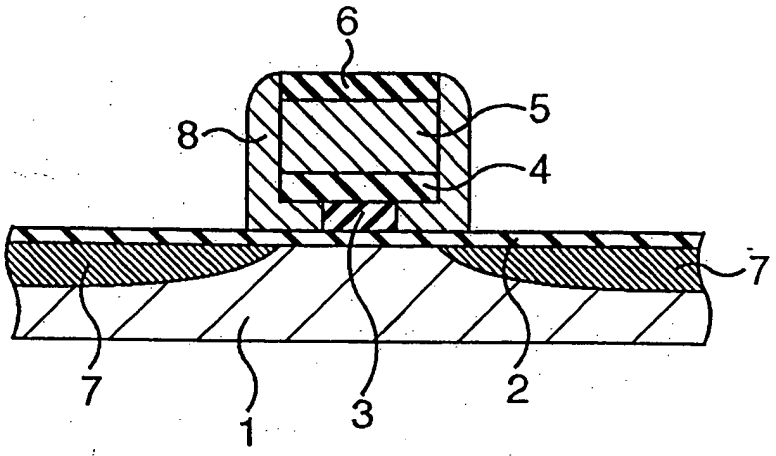


FIG. 1E

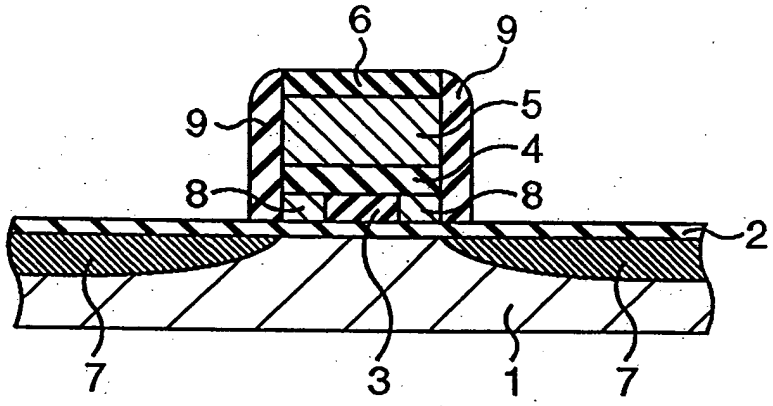


FIG. 1F

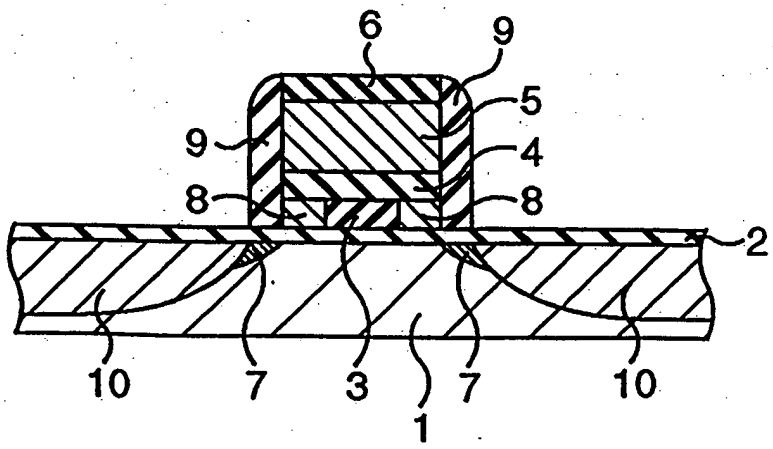


FIG. 2

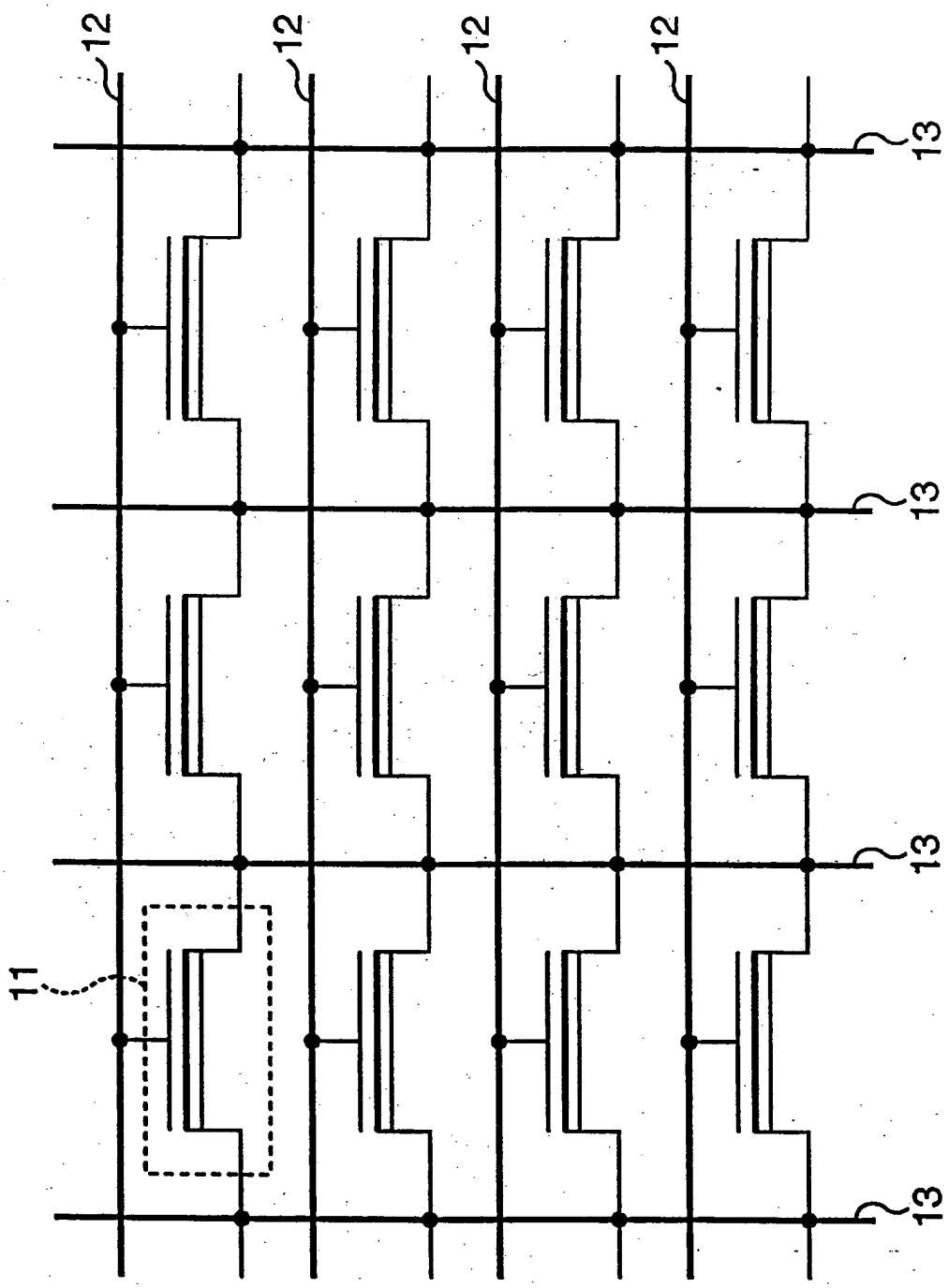
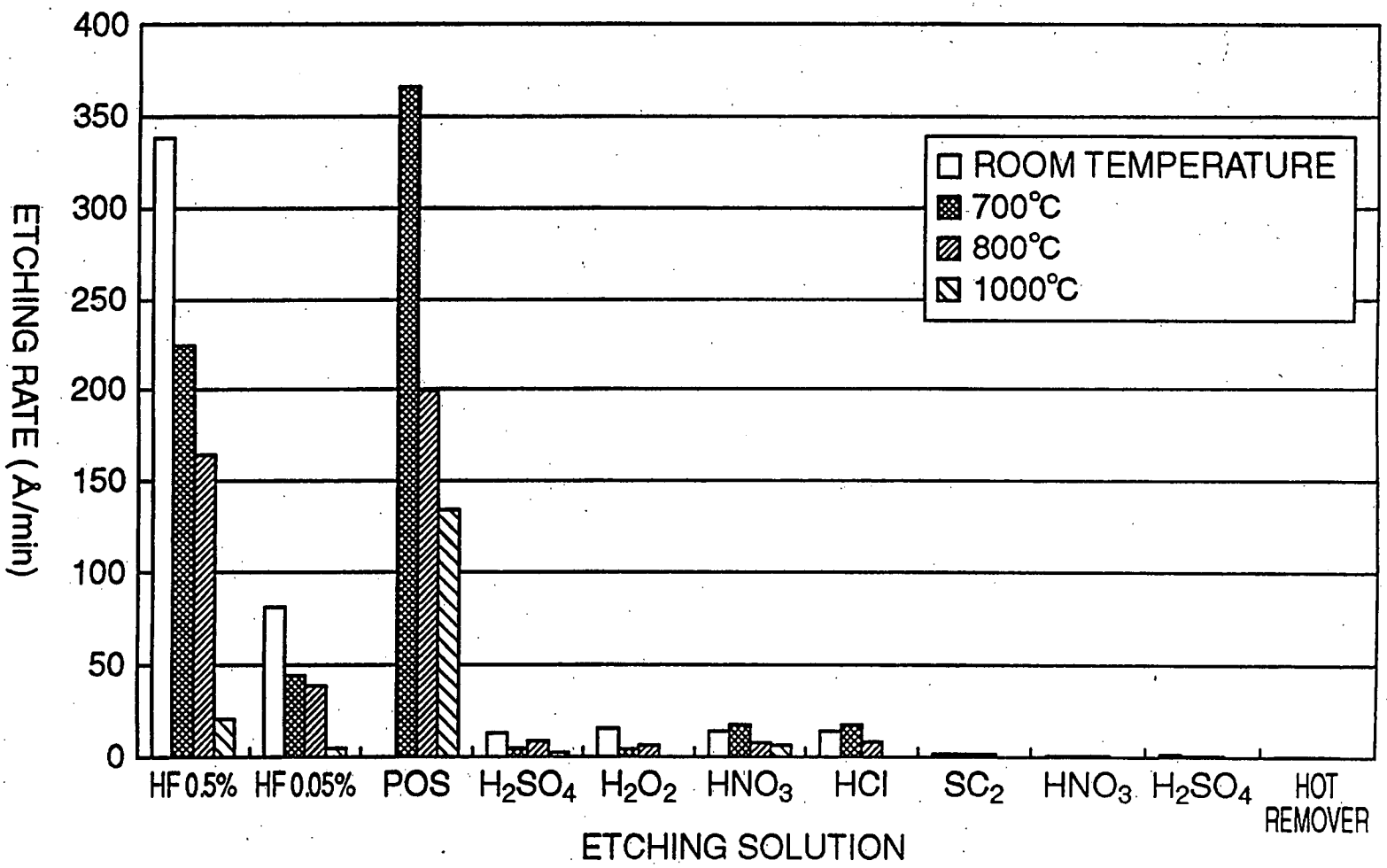


FIG. 3


400
350
300
250
200
150
100
50
0
ETCHING RATE (Å/min)
ROOM TEMPERATURE
700℃
800℃
1000℃
HF 0.5%
HF 0.05%
POS
H_2SO_4
H_2O_2
HNO_3
HCl
SC_2
HNO_3
H_2SO_4
HOT REMOVER
ETCHING SOLUTION

Necessary information for the missing inventor

1) The missing inventor: Masaki ISHIDAO

2) His last known address:

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3) The pertinent facts:

Declaration and Power of Attorney, Assignment, along with a copy of the present application were sent to the missing inventor's above address, requesting him to sign on the above documents and return to us, on September 22, 2004 via registered mail. However, the mail returned to us on October 1, 2004, since there was no one at the address. In addition, we have made efforts to locate him by using telephone directories, however his telephone number was unable to obtain since the telephone number with the above address was not registered. Accordingly, he can not be reached and it is impossible to obtain his signature on the Declaration and Power of Attorney as well as Assignment.

Nov. 2. 2004

Yasuko Soga

Yasuko SOGA
Patent Administration Department
FUJITSU LIMITED